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Study and Characterization of a New Trapezoidal Channel MOSFET for Negative Resistance Applications

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ABSTRACT. MOSFET transistors may be fabricated with a variety of gate geometries. The trapezoidal shape provides a new interesting one. If this non-standard geometry is made dependent on the biasing conditions, original behaviour and new I-V characteristics are expected to be obtained. This paper presents a study and characterization of this new device and shows that it provides a voltage controlled negative resistance. It is seen to have many noticeable advantages over those devices which are already known..

1. Introduction

In the last ten years, solid state scientists gave great attention to and struggled to realize a negative resistance device which is easy to control and reliable when used in original VLSI Applications[1-3]. They realized quickly that negative resistance devices were neither easy to control nor usable in many applications[2]. These devices were not compatible with the MOS/VLSI technology[2,4]. They were also associated with serious draw backs. Bad reproducibility, instability, narrow dynamic region of operation (some millivolts, some milliamperes) and bad noise figures are examples of drawbacks which made it difficult to use these devices without considerable precautions[2,4,6]. The paper presents a new MOSFET negative resistance device which is free from the majority of drawbacks of those devices which are already known. It incorporates a trapezoidal channel MOSFET which is so designed that the channel form is bias dependent. An original technique is employed which makes the channel width close to the drain decrease as the drain voltage V_{DS} increases.

Section 2 explains the construction and presents the theory of operation and modeling of the new negative-resistance trapezoidal-channel MOSFET (NRTC MOSFET). Experimental and simulation results are given in section 3. Discussion and conclusions are finally debated in section 4.

2. Theory of Operation and Modeling

This section comprises presentation of the new negative-resistance device construction and its theory of operation. It also develops analytical modeling for evaluating the device characteristics and predicting its performance.

2.1 Construction and Theory of Operation

The new negative-resistance trapezoidal-channel MOSFET is constructed as shown in Fig. (1) of a rectangular gate MOSFET with L, Z and d_0 being the channel length, width and depth respectively, h_o is the oxide layer thickness. A semitriangular floating gate piece FG is introduced below the control gate CG close to the drain. The height and base length of the rectangular part of the floating gate piece are Δl_D and Z respectively. This piece is charged to a certain potential ΔV_F. When the MOSFET is switched into saturation ($V_{DS} \geq V_{GS} - V_T$) and pinch-off is to occur, the potential at the edge of the source-region of the channel close to the drain should be equal to $V_{GS} - V_T$ even if V_{DS} is increased, further, to values greater than $V_{DS} = V_{GS} - V_T$. However channel regions lying below the semitriangular floating gate piece acquire potential equal to $V_{GS} + \Delta V_F - V_T$ which is still greater than the value needed to establish pinch-off near the drain. As a consequence, pinch-off does not take place beneath the floating gate piece (over a width Z') while occurring elsewhere. The channel current stream accommodates itself in a trapezoidal formed channel and drain widths Z and Z' respectively.

As V_{DS} is increased over its saturation value ($V_{DSS} = V_{GS} - V_T$), the source-region channel length L_s shrinks back, while the length Δl of the pinch-off region increases. As a result the effective drain width of the channel Z' decreases and the channel current will be forced to undergo a more steeper trapezoidal stream.

As will be shown later, the MOSFET saturation current is expected to decrease as V_{DS} is increased (due to decreasing of the drain channel Z'). This means that the I-V characteristic acquires a negative slope which indicates that the presented devide provides a negative resistance.

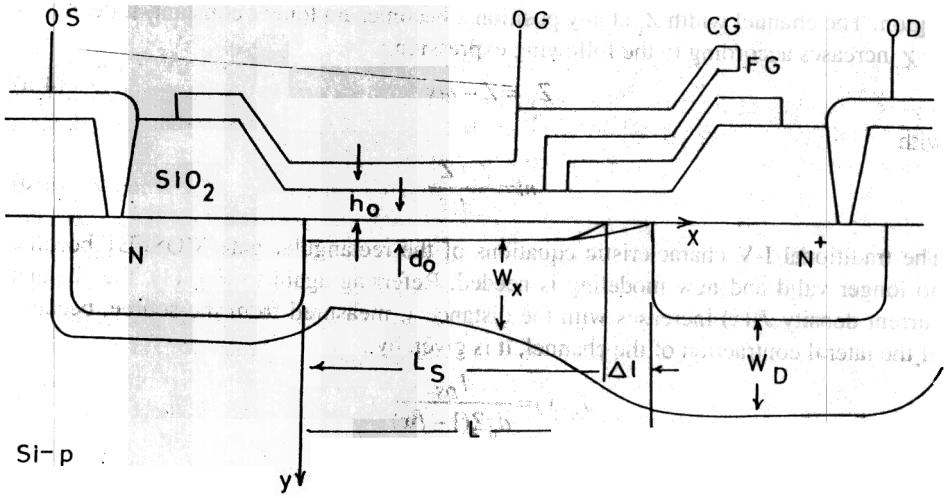
2.2 Model

Referring to Fig. (1) where the NTRC MOSFET is shown with the coordinate system, x, y, z. The pinch-off region length Δl depends, in fact, on the device biasing voltages V_{DS}, V_{GS} and geometry L, h_0 and d_0. We have shown in other publications[7,8] that Δl is given by :

$$\Delta l = \left(\frac{9\varepsilon_s d_0 h_0 L}{4\varepsilon_0} \right)^{\cdots} \left(\frac{V_{DS}}{V_{DSS}} - 1 \right)^{\cdots} \tag{1}$$

with ε_s and ε_0 being the silicon and oxide permittivities respectively. Equation (1) shows that Δl increases proportionally with the drain voltage V_{DS} as long as it is greater than the drain saturation value V_{DSS}. The drain channel-width Z' is seen to decrease as Δl increases (or in other words as V_{DS} increases). It could be formulated by :

$$Z' = Z\left| 1 - \frac{\Delta l}{\Delta l_F} \right) \tag{2}$$



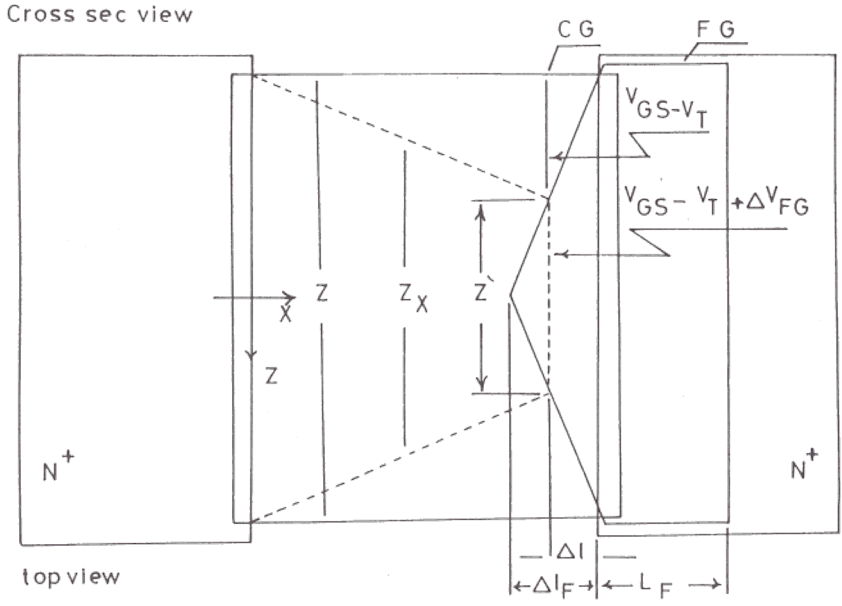


FIG. Cross sectional and top view of trapezoidal channel MOSFET.

Substituting equation (1) into equation (2) yields,

$$Z' = Z\left[1 - \frac{1}{\Delta l_F}\left(\frac{9\varepsilon_s d_0 h_0 L}{4\varepsilon_0}\right)^{2/3}\left(\frac{V_{DS}}{V_{DSS}} - \right)^{2/3}\right] \tag{3}$$

The channel form becomes trapezoidal as the MOSFET is switched into its saturation region. The channel width Z_x at any position x becomes no longer constant. It decreases as χ increases according to the following expression :

$$Z_x = Z - mx \tag{4-a}$$

with

$$m = \frac{Z - Z'}{L} \tag{4-b}$$

The traditional I-V characteristic equations of the rectangular gate MOSFET become no longer valid and new modeling is needed. Referring again to Fig. (1), the channel current density $J_n(x)$ increases with the distance x, measured from the source, because of the lateral contraction of the channel, it is given by :

$$J_n(x) = \frac{I_{DS}}{d_0 Z(1 - \beta x)} \tag{5-a}$$

with

$$\beta = \frac{m}{Z} = \frac{1}{L}\left(1 - \frac{Z'}{Z}\right) \tag{5-b}$$

The channel current I_{DS} can be written as[9,10]

$$I_{DS} = \int_0^{\infty} qn(y)\mu_n(x,y)E_x(x)Z_x dy$$

multiplying and dividing by $Q_n = \int_0^{\infty} qn(y)dy$ yields[8,9].

$$I_{DS} = Q_n \mu_n(x) E_x Z_x \tag{6}$$

Since the total MOS system is charge neutral,

$$Q_G + Q_{SS} + Q_n + Q_B = 0 \tag{7}$$

where Q_G, Q_{SS}, Q_n and Q_B are the charges at the gate, the interface states, the channel inversion layer and the bulk depletion region respectively. Q_n can be formulated by[2,5]

$$Q_n = -C_{ox}[V_{GS} - V_T - V_x] \tag{8-a}$$

with

$$Q_G = C_{ox}(V_{GS} - V_x)$$

and

$$V_T = -\frac{Q_{ss}^{+} + Q_B^{-}}{C_{ox}} \tag{8-c}$$

Substituting equation (4) and (8) into equation (6) and replacing E_x by $-\frac{dV_n}{dx}$ yields.

$$\frac{I_{DS}dx}{Z(1-\beta x)} = C_{ox}\mu_n(x)(V_{GS} - V_T - V_x)dV_x \tag{9}$$

The channel field E_x is enhanced in the contracted parts of the channel due to the enhancement of the channel current density ($E_x = J_n(x)/\sigma$, with σ being the channel conductivity). The channel mobility degradation due to high field operation should, therefore, be taken into account. This effect becomes appreciably important when E_x exceeds a certain critical value E_c(~ 1.5 V/μ for electrons and $2V/\mu$ for holes)[7,11]. The value of the channel mobility becomes position dependent. It is given by :

$$\mu_n(x) = \mu_n \sqrt{E_c / \frac{dV_x}{dx}} \tag{10}$$

Combining equations (9) and (10) yields

$$\frac{I_{DS}^2 dx}{Z^2(1-\beta x)^2} = C_{ox}^2 \mu_n^2 E_c (V_{GS} - V_T - V_x)^2 dV_x \tag{11}$$

To obtain I_{DS} the left term of equation (11) should be integrated along the length of the channel from $x = 0$ to $x = L$ and the right term should be integrated between corresponding voltage limits $V_x = 0$ to $V_x = V_{DS}$;

$$\frac{I_{DS}^2}{Z^2}\int_0^L \frac{dx}{(1-\beta x)^2} = C_{ox}^2 \mu_n^2 E_c \int_0^{V_{DS}} (V_{GS} - V_T - V_x)^2 dV_x$$

from which

$$I_{DS} = C_{ox}\mu_n \frac{Z}{L}\sqrt{(1-\beta L)V_c V_g}\sqrt{V_g V_{DS} - V_{DS}^2 + \frac{V_{DS}^3}{3V_g}}$$

Substituting equations (3) and (5) into equation (12) yields,

$$I_{DS} = \alpha\sqrt{V_g V_{DS} - V_{DS}^2 + \frac{V_{DS}^3}{3V_g}}, \quad V_{DS} < V_g$$

$$I_{DS} = \alpha\sqrt{1 - k\left(\frac{V_{DS}}{V_{DSS}} - 1\right)^{2/3}}\sqrt{V_g V_{DS} - V_{DS}^2 + \frac{V_{DS}^3}{3V_g}}, \quad V_{DS} > V_G \tag{13-b}$$

with

$$V_g = V_{GS} - V_T$$

$$\alpha = C_{ox}\mu_{ox}\frac{Z}{L}(V_c V_g)$$

$$k = \frac{1}{\Delta l_F}\left(\frac{9\varepsilon_s d_0 h_0 L}{4\varepsilon_0}\right)^{1/3}$$

and

$$V_c = E_c L$$

Equations (13-a,b) show that I_{DS} increases, in the ohmic region ($V_{DS} < V_g$), proportionally as V_{DS} increases. However the rate of increase of I_{DS} and V_{DS} will be smaller than that observed with traditional rectangular gate MOSFETs. This is referred to the channel field enhancement and the consequent degradation of the channel carrier mobility. In the saturation region of operation, I_{DS} decreases as V_{DS} is increased because the channel width Z' at the drain decreases as increasing V_{DS}. The I-V characteristics are expected, therefore, to have negative slopes, which means that the device acquires a negative resistance. The sensitivity of the drain channel width Z' to variations in V_{DS}, during the operation of the MOSFET in saturation, is seen to be dependent on the geometry of the floating gate-piece. The device's negative resistance will also be controllable via control of the floating gate-piece geometry.

3. Experimental and Simulation Results

The experimental work begins by preparing trapezoidal gate N-channel test MOSFETs. The source channel-width $Z = 50\mu m$, the drain channel-width Z' ranges from 5 to $50\mu m$, channel length $L = 5\mu m$ and oxide thickness h_0 ranges from 40 to 1200Å. Measurements are performed on these test specimens to obtain the value of the effective MOSFET geometrical ratio $(Z/L)_{eff}$ and its dependence on the device geometry (Z,L,β) and biasing (V_{DS} , V_{GS}). Figure (2) shows a photomicrograph of the trapezoidal gate test devices. Figure (3) presents the variation of the effective value of the geometrical ratio $(Z/L)_{eff}$ with the drain channel-width Z' as deduced from the presented model (Equation 13a,b) and compares it to experimental measurements. A good agreement is observed between the theory and experiment.

The variation of Z' with $\frac{V_{DS}}{V_{DSS}}$ is evaluated using equation (3). As Fig. (4) shows, Z' decreases as the value of $\frac{V_{DS}}{V_{DSS}}$ increases. It will be easy to conclude that the effective value of the geometrical ratio $(Z/L)_{eff}$ also proportionally decreases as $\frac{V_{DS}}{V_{DSS}}$ increases.

The experimentally determined values $(Z/L)_{eff}$ are fed to a simulation program based on the proposed model and used to evaluate the I-V characteristics of the presented NR-device. As shown in Fig. (5), when the NR-device is operated in its ohmic region, I_{DS} seen to increase as V_{DS} increases. However, when the device is switched into its saturation region I_{DS} decreases as V_{DS} increases. This means that the I-V curves undergo a negative slope, which indicates that the device has a negative resistance. The value of this resistance is dependent on the sensitivity of Z'' to the variation of V_{DS}. This latter can be varied by varying the geometry of the floating gate piece (See Figs. (1) and (4)).

Figure (5) shows the variation of the device's negative resistance V_{DS} with the gate voltage V_{GS}. We observe that the amplitude of V_{DS} first decreases sharply as V_{GS} increases. Afterwards $V_{GS} > 5V$) the decrement of r_{DS} with V_{GS} becomes small. We also notice that the amplitude of V_{DS} is dependent on the shape and geometry of the floating gate piece.

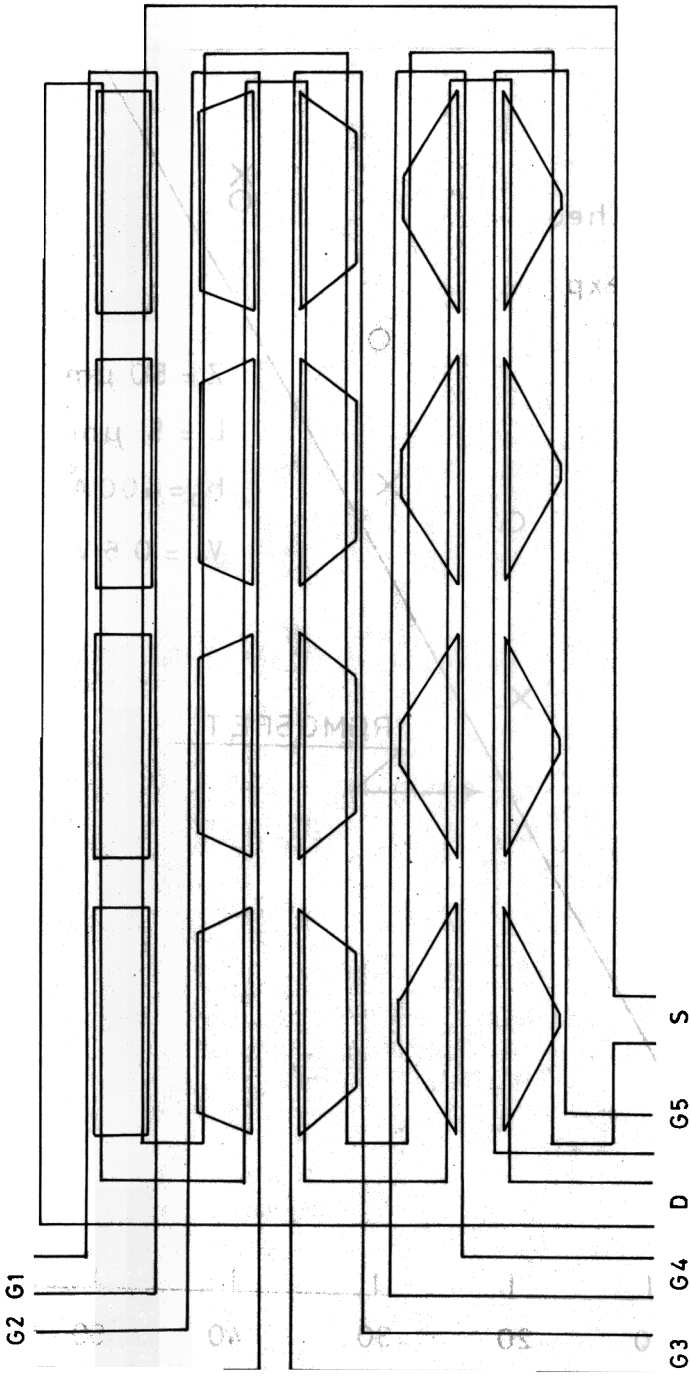


FIG. 2. Photomicrograph of the trapezoidal gate test device.

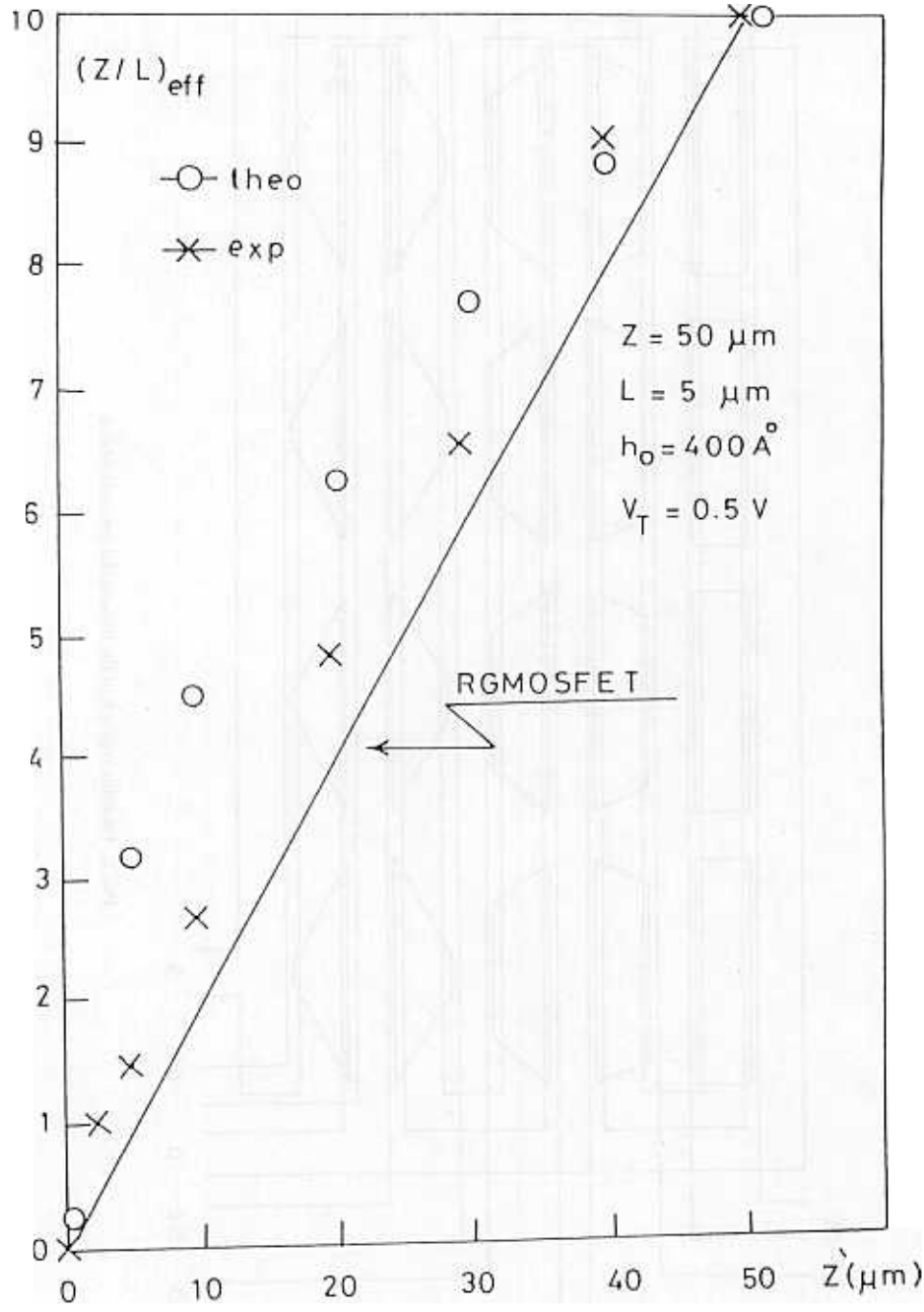
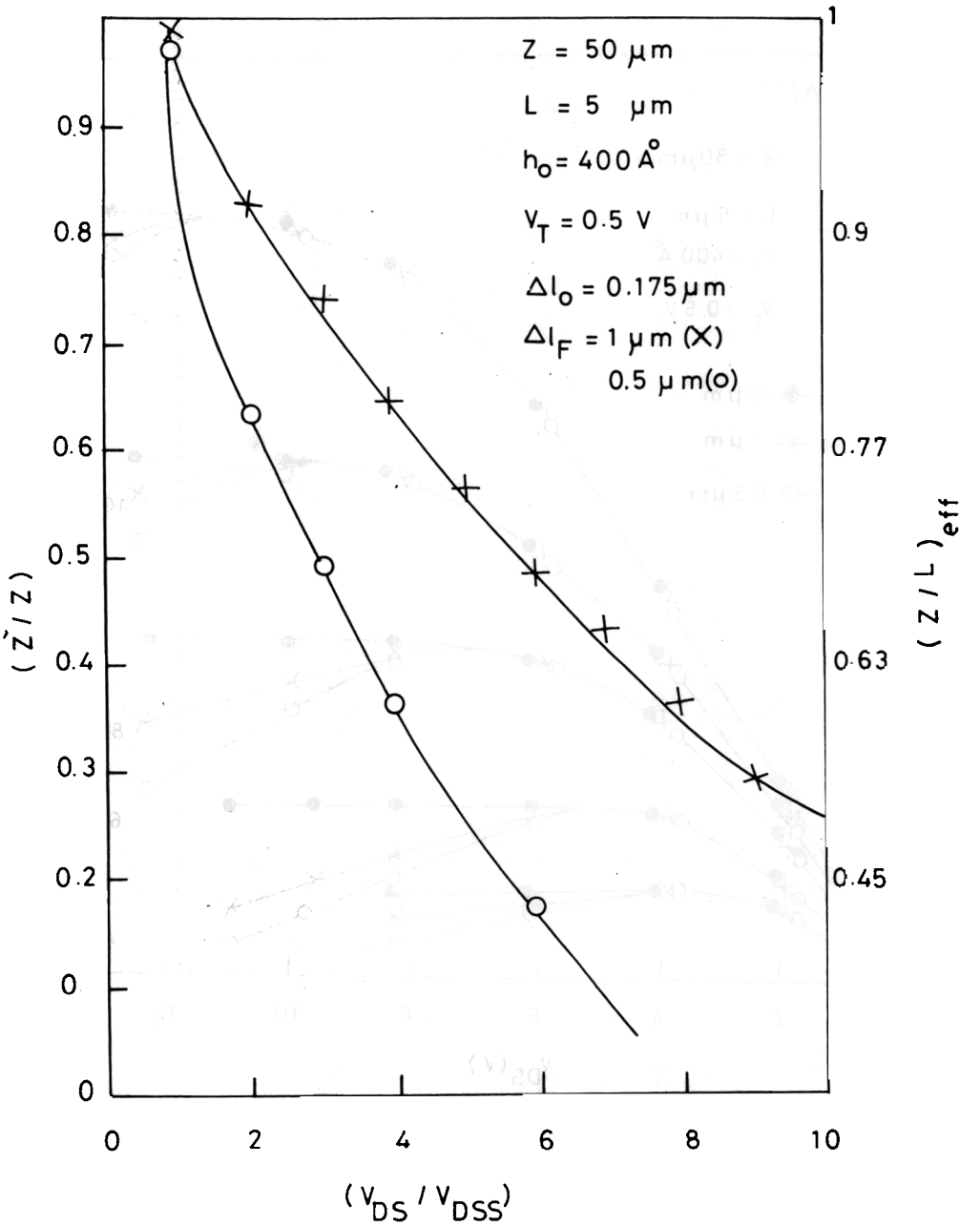


FIG. 3. Variation of geometrical ratio *Z/L* with drain channel width *Z*.



Variation of Z'/Z and V_{DS}/V_{DSS}

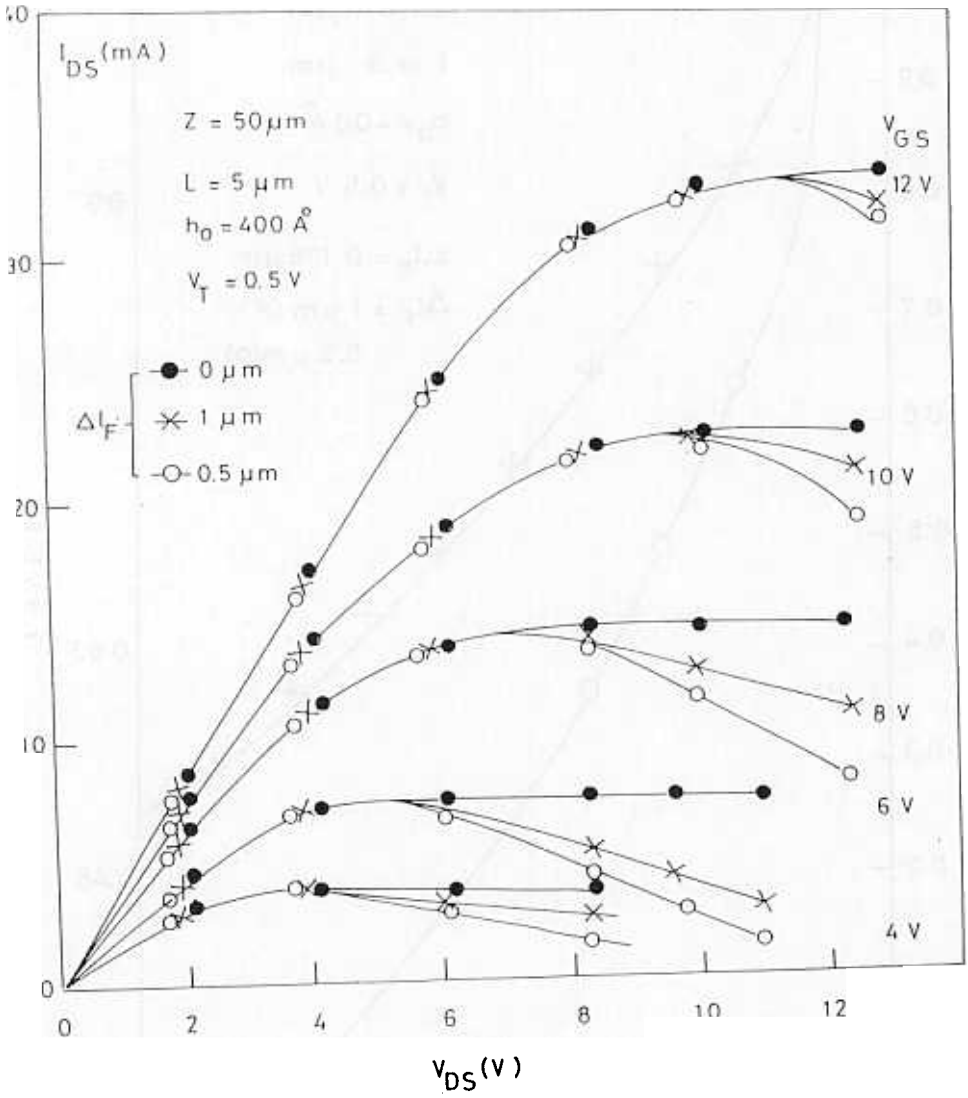


FIG. 5. Variation of I_{DS} and V_{DS}.

4. Conclusions

A new negative resistance device is presented. It is found to be free from the majority of drawbacks of those traditional devices which are already known. The new device is to be integrated using the floating gate MOSFET technology. The negative resistance manifested by the presented device is shown to depend on the floating gate shape and geometry and its value can be adjusted, during device operation, by adjustment of the gate to source voltage V_{GS}. The theory of operation of this device is experimentally verified by integrating a large number of rectangular gate test MOSFETs of different channel lengths and gate side steepness, and measuring the effective value of their geometrical ratios $(Z/L)_{eff}$. The model of simulation takes into account the mobility degradation resulting from the carrier heating occurring due to channel field enhancement. Then new device is needed in many applications. It is quite easy to use without serious precautions.

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دراسة ونمذجة وصلة كهربائية من الـ MOSFET لاستخدامها في التطبيقات المتعلقة بالمقاومات الكهربائية السالبة

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المستخلص . كما هو معروف إن هذه الوصلات الكهربائية المستخدمة في الأجهزة الإلكترونية يمكن تطبيقها على أشكال مختلفة وبأحجام متغيرة حسب استخداماتها التطبيقية وهذه القطعة التي هي موضوع البحث المقدم والمسماة (TRAPEZOIDAL) تعتبر من أهم هذه الوصلات الكهربائية - وقد عملت هذه الوصلة بطريقة جديدة من أجل الحصول على العلاقة ما بين التيار الكهربائي والجهد المستخدمة في تطبيقات الـ (VLSI) حيث إنه يمكن التحكم في الجهد الكهربائي حتى نستطيع أن نحصل على المقاومة الكهربائية السالبة .

وكما يتضح في موضوع البحث إن هذا النوع من الوصلات الكهربائية سوف يكون لها عدة مميزات في حالة تطبيقها لتكون بديلاً لما هو موجود حاليًا ومستخدمًا في هذا المجال التقني وذلك لسهولة تطبيقها وكذلك استخداماتها .