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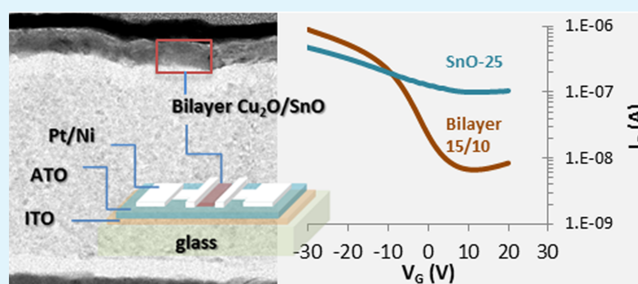
P-Type Cu_2O/SnO Bilayer Thin Film Transistors Processed at Low Temperatures

Hala A. Al-Jawhari,[†] Jesus A. Caraveo-Frescas,[‡] M. N. Hedhili,[‡] and H. N. Alshareef*[,‡]

[†]Department of Physics, King Abdulaziz University, Jeddah 21589, Saudi Arabia

[‡]Materials Science and Engineering, King Abdullah University of Science and Technology (KAUST), Thuwal 23955-6900, Saudi Arabia

ABSTRACT: P-type Cu_2O/SnO bilayer thin film transistors (TFTs) with tunable performance were fabricated using room temperature sputtered copper and tin oxides. Using Cu_2O film as capping layer on top of a SnO film to control its stoichiometry, we have optimized the performance of the resulting bilayer transistor. A transistor with 10 nm/15 nm Cu_2O to SnO thickness ratio (25 nm total thickness) showed the best performance using a maximum process temperature of 170 °C. The bilayer transistor exhibited p-type behavior with field-effect mobility, on-to-off current ratio, and threshold voltage of 0.66 $cm^2\ V^{-1}\ s^{-1}$, 1.5×10^2, and −5.2 V, respectively. The advantages of the bilayer structure relative to single layer transistor are discussed.



KEYWORDS: *thin film transistor, tin monoxide, cuprous oxide, bilayer channel, oxide semiconductors*

■ INTRODUCTION

Tin monoxide (SnO) and copper oxide (Cu_2O) are the two most promising p-type transparent oxide semiconductors because of their native polarities, which have been attributed to contributions from Sn 5s and Cu 3d states near their valence band maxima (VBM).[1−3] Both oxides have shown encouraging performance in p-type thin-film transistors (TFTs).[4−9] A detailed progress concerning this topic was recently reported by E. Fortunato et al.[10] However, the current performance of p-type oxides is not yet satisfactory for commercial applications, and more progress must still be made in their performance to realize any real applications.

A common feature between all reported SnO TFTs is the large off-current and the depletion mode operation.[3,4,11,12] Such characteristics were ascribed to the high hole density in the SnO films, which depends primarily on both deposition and post annealing conditions. Since all as-deposited SnO films produced at room temperature are amorphous, an anneal step is required to crystallize the films. Yet, post-annealing has a strong influence on the chemical composition and electrical transport properties of the resulting SnO film. As a metastable phase, SnO can be easily oxidized during annealing in air and transformed into n-type Sn_3O_4 or SnO_2. At lower temperatures, 140 °C ≤ T < 200 °C, such oxidation occurs mainly at the exposed surface of SnO by chemical reactions involving surface adsorbed oxygen atoms.[13] This reaction can increase oxygen concentration near the SnO surface, and since O interstitials can be ionized to yield two holes and interstitial O^{2-} oxygen ions,[3] such process may increase the total holes density in SnO, and hence the film electrical conductivity. With a further increase in temperature, 200 °C ≤ T < 300 °C, an internal oxidation process occurs due to the localized disproportionate redistribution of oxygen in SnO film. This internal oxidation process can lead to the formation of metallic tin, Sn_3O_4, or SnO_2. The existence of small metallic tin precipitates and n-type SnO_2 crystallites in a p-type α-SnO film will reduce both the concentration and the mobility of electrical carriers in the SnO film.[13] Therefore, adjusting the amount of excess oxygen during post-deposition annealing of SnO is so crucial not only for controlling the crystallization and formation of the desired phase of tin oxide but also for achieving the optimal amount of carrier density and off-current, while keeping an appropriate hole mobility.

To control oxygen penetration into and out of SnO films during annealing process, Yabuta et al.[11] have employed silica (SiO_2) capping layers on top of their sputtered SnO thin films. Their study demonstrated that SnO-based TFTs annealed at T ≥ 300°C without capping layers exhibit n-type behavior, even when annealed in N_2 atmosphere. While those with SiO_2 capping layers exhibited p-type performance with an on/off ratio (I_{on}/I_{off}) and field effect mobility of 10^2 and 0.24 $cm^2\ V^{-1}\ s^{-1}$, respectively. Nonetheless, their device off-current (I_{off}) was relatively high $\sim10^{-7}$ A.

In this study, we have evaluated Cu_2O instead of SiO_2 as capping layer for SnO thin film transistors. Since Cu_2O is also a p-type semiconductor, it can act not only as capping layer of SnO to control its oxygen stoichiometry but also possibly improve the overall performance of the device using a stacked

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channel scheme. In fact, the Cu_2O phase is known to be quite stable within certain temperature and oxygen pressure range and certainly more stable than SnO.[14,15] Thus, using Cu_2O as a capping layer on top of SnO could moderate oxidation of the exposed surface of the active SnO channel, which in turn, may reduce the surface leakage current that usually increases the device off-current. Another potential advantage of using Cu_2O as capping layer is its tendency to give up oxygen to certain oxide films that come in direct contact with it.[14,16] This feature of Cu_2O may be exploited in Cu_2O/SnO bilayer stacks to enhance oxidation of the adjacent SnO films, possibly reducing the required annealing temperature.

■ EXPERIMENTAL SECTION

Cu_2O/SnO bilayer TFTs were built according to our baseline process, which uses 220 nm aluminum titanium oxide (ATO) dielectric deposited on a glass-coated with a 150 nm indium tin oxide (ITO) gate electrode. Both copper oxide and tin monoxide films were deposited by reactive DC magnetron sputtering at room temperature using metallic Sn and Cu targets. SnO films were deposited first as bottom layers using deposition pressure, total gas flow (Ar + O_2), and dc power of 1.8 mTorr, 20 sccm, and 20 W, respectively. To evaluate the optimal conditions for the bilayer stacks, deposition was repeated at four different relative oxygen partial pressures (O_{pp}): 0%, 3%, 5%, and 9%. The Cu_2O films were then deposited on top of SnO using previously optimized deposition conditions including O_{PP} of 10%, deposition pressure of 4.5mTorr, and dc power of 50 W. For source-drain contacts, electron-beam evaporated Pt/Ni contacts were used, since they form ohmic contacts with both Cu_2O and SnO layers.[5,11,17] The Ni was in contact with the Cu_2O film. Various channel thicknesses ($t_{Cu_2O} + t_{SnO}$) with different thickness ratios (t_{Cu_2O}/t_{SnO}) were utilized to fabricate several sets of bottom gate bilayer p-type TFTs. Both the bilayer channel and the source-drain electrodes were patterned by lift-off photolithography. The width-to-length ratio (W/L) of all measured devices were $W/L = 1$, with $L = 100\mu$m. A schematic illustration of the bilayer transistor prototype is shown in Figure 1a. All final devices were subject to post annealing at temperatures between 140 and 190 °C for 30 minutes in air using a tube furnace. A Keithley 4200-SCS precision semiconductor parameter analyzer was used to measure the electrical transport properties of TFTs. All electrical measurements were performed in the dark at ambient temperature. Linear field-effect mobility (μ_{FE}) and threshold voltage (V_T) were extracted from the ($I_D - V_G$) transfer characteristics, while subthreshold swing (SS), which is defined as $SS = [\partial V_G/\partial \log (I_D)]$, was evaluated using the slope of the weak-region of ($\log (I_D) - V_G$) plot, where $V_G < V_T$. The maximum number of traps D_{it} at the oxide/dielectric interface was then estimated as $D_{it} = [((SS \log(e))/(KT/q))-1](C_{ox}/q)$ where $C_{ox} = 55$ nF cm^{-2} is the capacitance of the gate dielectric. Microstructures, bonding environment, and optical transmission characteristics of the deposited bilayer channels were characterized by transmission electron microscopy (TEM), X-ray photoelectron spectroscopy (XPS), and UV−vis spectrophotometry.

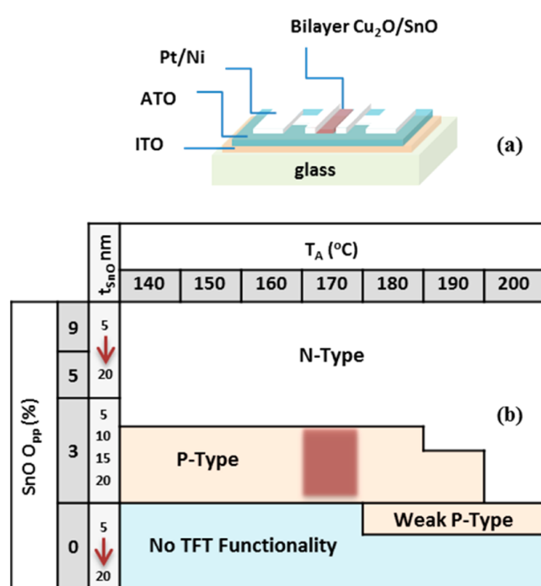

Figure 1. (a) Schematic diagram of the bilayer TFT device and (b) process map showing Cu_2O/SnO bilayer TFT polarity obtained under different oxygen partial pressures (O_{pp}) and anneal temperatures.

■ RESULTS AND DISCUSSION

The first set of Cu_2O/SnO bilayer TFTs were fabricated using our two best deposition conditions for both films, which were 10% O_{pp} for Cu_2O and 9% O_{pp} for SnO.[12] Such conditions consistently give p-type TFT behavior in our single layer TFTs. However, unexpectedly, all bilayer devices exhibited n-type behavior regardless of the (t_{Cu2O}/t_{SnO}) ratio or annealing temperature. The most likely explanation for this surprising behavior is that oxygen from the 10% O_{pp} Cu_2O was lost to SnO film, transforming the 9% O_{pp} SnO layer into the SnO_2 phase at temperatures as low as 160°C. It has been previously reported[13] that transforming SnO film to n-type SnO_2 by annealing in air required temperatures as high as 300°C. However, in the bilayer case, we surmise that not only we do have oxygen from air, but also from the Cu_2O film that is in contact with SnO. Hence a lower SnO to SnO_2 transformation temperature was observed.

To avoid the SnO to SnO_2 transformation at such low temperatures, we employed oxygen-poor SnO films instead of the stoichiometric ones. Keeping the O_{pp} used for deposition of Cu_2O upper layer at a constant value of 10%, a value that gives good p-type behavior in our Cu_2O films, we varied the O_{pp} used during the deposition of SnO films from 0 to 5% (O_{pp} = 5%, 3%, and 0%) and fabricated a matrix of Cu_2O/SnO bilayer TFTs. To adjust the oxidation of SnO more precisely, and optimize bilayer device performance we evaluated several thickness ratios (t_{Cu2O}/t_{SnO}) and several total thickness ($t_{Cu2O} + t_{SnO}$) values of Cu_2O/SnO bilayer transistors. These experimental variations are summarized in Figure 1b. The summary in Figure 1b shows that with a 10% O_{pp} Cu_2O as a capping layer, a SnO film of at most O_{pp} = 3% is required to achieve p-type Cu_2O/SnO bilayer transistor behavior. When a tin monoxide layer with relative oxygen pressure above 3% is used, the SnO film is transformed into SnO_2 showing n-type behavior. This observation is likely due to the fact that additional oxygen diffusion from the 10% O_{pp} Cu_2O layer into the underlying SnO film (O_{pp} > 3%), leading to the formation of n-type Sn_3O_4 or SnO_2.

In contrast, when Sn metal is used as first layer (0% O_{pp} deposition from Sn metal target), no TFT functionality is observed except some weak p-type behavior at higher temperatures (≥ 180 °C). This is because p-type behavior in the Cu_2O/Sn stack requires a supplementary amount of oxygen that is more than can be delivered by the 10% O_{pp} Cu_2O capping film. One can also notice in Figure 1b that the thickness of metallic Sn is important for bilayer TFT functionality. Weak p-type behavior by the Cu_2O/Sn stack is only obtained for rather thin Sn films (5−10 nm). As Sn metal thickness increases, it becomes increasingly difficult to oxidize the entire Sn film by oxygen diffusion from Cu_2O, and the weak p-type behavior disappears. However, since the TFT perform-

ance of such films (Cu_2O on 0% O_{pp} Sn) was not good, no further analysis was carried out on these devices.

Finally, Figure 1b shows that using metal-rich SnO_x films deposited at 3% O_{pp}, the Cu_2O/SnO_x bilayer TFTs that show p-type behavior can be obtained over a wide range of stack annealing temperatures (140−190 °C), with a best condition at 170 °C anneal temperature. Yet, even with 3% O_{pp} SnO deposition, all devices with thin SnO layer (t_{SnO} = 5 nm) showed an n-type behavior irrespective of the thickness of the Cu_2O above. This observation is consistent with the previous assumption that the Cu_2O layer provides additional oxygen that increases the oxidation rate of the metal-rich SnO layer underneath. The thinner the SnO layer, the less the number of pure Sn atoms that exist, and hence, a complete oxidation by the oxygen diffusion from the Cu_2O layer is expected. Therefore, unless we use a thicker SnO film with a higher percentage of metallic Sn, the right phase of SnO for p-type process would not form. Trying three other thicker layers of the 3% O_{pp} SnO films (10, 15 and 20 nm), covered with three different thicknesses of Cu_2O layers (5, 10, and 20 nm), we found that the condition of t_{Cu2O}/t_{SnO} = 10/15 annealed at 170 °C for 30 min in air provides the optimum device performance.

For better understanding of the behavior of Cu_2O/SnO bilayer TFTs, we compared the bilayer TFT performance to single layer TFTs fabricated using only SnO film (25 nm) deposited using O_{pp} of 3%. Figure 2a−c shows the $I-V$ characteristics of the 25 nm-SnO single layer and two different Cu_2O/SnO bilayer TFTs. The bilayer TFTs had the same total thickness ($t_{Cu_2O} + t_{SnO}$ = 25 nm) as the single layer TFT (SnO = 25 nm), but with different ratios: t_{Cu2O}/t_{SnO} = 10/15 and t_{Cu2O}/t_{SnO} = 5/20. All films were annealed for 30 min at 170 °C in air. For both bilayer TFTs, as the gate voltage V_G decreased

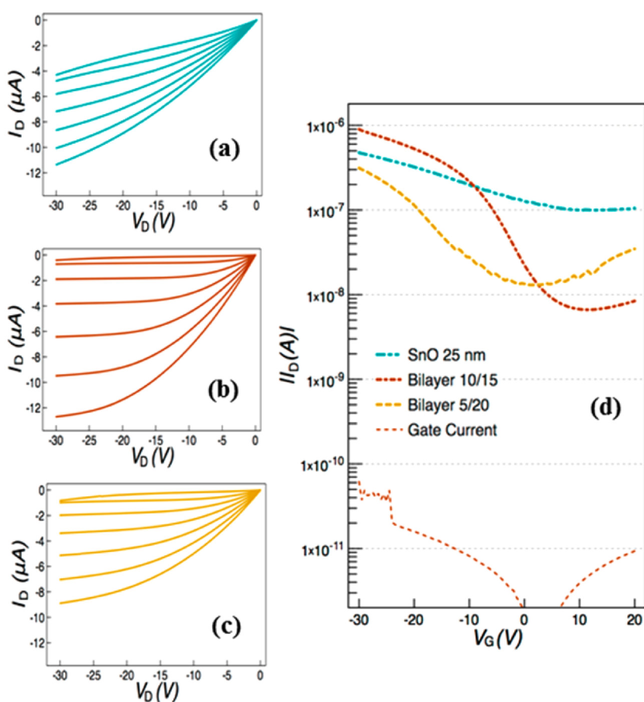

Figure 2. Output characteristics of (a) single layer 25 nm SnO TFT, (b) 10/15 bilayer, and (c) 5/20 bilayer TFTs. For all cases, V_G was swept from 0 to −30 V by a step of −5 V. (d) Transfer curves of the three previous TFTs at V_D = −1 V and the gate-leakage current of the 10/15 bilayer TFT.

from 0 to −30 V, the drain current I_D showed a clear modulation, indicating that the Cu_2O/SnO bilayer TFTs were working as p-channels controlled by the gate and drain bias. On the other hand, the characteristics of the 25 nm SnO TFT showed a high I_{off} and a lack of saturation, a performance that may be attributed to the presence of high carrier density in the channel becauseo of the surface oxidation as mentioned previously. Figure 2d shows the transfer curves for the same three devices at a fixed drain voltage of V_D = −1 V. Consistent with the common feature of SnO based TFTs, our 25 nm-SnO TFT exhibited positive threshold voltage (V_T = 5.2 V), high I_{off} (~1×10^{-7}A), and a field effect mobility of μ_{FE} =0.23 cm²/(V s). One possible reason behind such relatively low mobility could be that the 170 °C was not high enough to complete the oxidation of this Sn-rich SnO layer, and thus stoichiometric SnO phase did not form. It is well known that the presence of metallic tin can introduce point defects or dislocations that scatter the carriers and, hence, reduce device mobility. The observed high values of subthreshold slope SS and density of trap states D_{it} for this TFT confirm this assumption. In contrast, the t_{Cu_2O}/t_{SnO} = 10/15 bilayer TFT processed at the same annealing temperature as the single layer TFT discussed above, exhibited an improved performance. The I_{off} current dropped by two order of magnitudes, the V_T showed a clear negative shift to (−5.2) V, the field-effect mobility increased to 0.66 cm²/(V s), and the extracted subthreshold swing decreased to 8.4 V/dec, clearly indicating the advantage of using Cu_2O capping layer. The bilayer TFT fabricated using t_{Cu_2O}/t_{SnO} = 5/20 showed an intermediate performance with a field-effect mobility, off-current, and threshold voltage of 0.39 cm²/(V s), 13 nA, and −14.9 V, respectively. We attribute this moderate performance to its thinner copper oxide layer and thicker SnO. The gate-leakage current of the t_{Cu_2O}/t_{SnO} = 10/15 bilayer TFT, which is on the order of 10^{-11} A, is also shown in Figure 2d. Similar gate leakage currents were obtained for the other two transistors. This indicates that the impact of gate leakage on the electrical performance of these devices can be ignored. A summary of the measured device parameters for these three TFTs are summarized in Table 1.

Table 1. Linear Field-Effect Mobility (μ_{FE}), Threshold Voltage (V_T), Off-Current (I_{off}), Subthreshold Swing (SS), and Maximum Number of Interface Traps (D_{it}) for the Monolayer SnO and the Two (10/15) and (5/20) Bilayer TFTs after Being Annealed at 170 °C in Air

TFT type	bilayer 10/15	bilayer 5/20	monolayer SnO-25
μ_{FE} (cm² V⁻¹ S⁻¹)	0.66	0.39	0.23
V_T (V)	−5.2	−14.9	5.2
I_{Off} (nA)	−6.63	−13.01	−99.7
SS (V/dec)	8.40	21.09	51.28
D_{it} ×10¹³ (eV⁻¹ cm⁻²)	4.85	12.2	29.8

To verify the chemical compositions of the 10/15 nm bilayer stack and identify the phase of each layer, (XPS) depth profile measurements were carried out, before and after being annealed for 30 min at 170°C in air. Measurements were taken at two different etching times for each layer based on its depth; specifically, 60 s and 180 s were used for Cu_2O and SnO layers, respectively. Etching was done using a 500 eV argon ion beam on sputter area of 2×2 mm at an etch rate of 5 nm/min. The change in the tin oxidation state was noticeable by monitoring

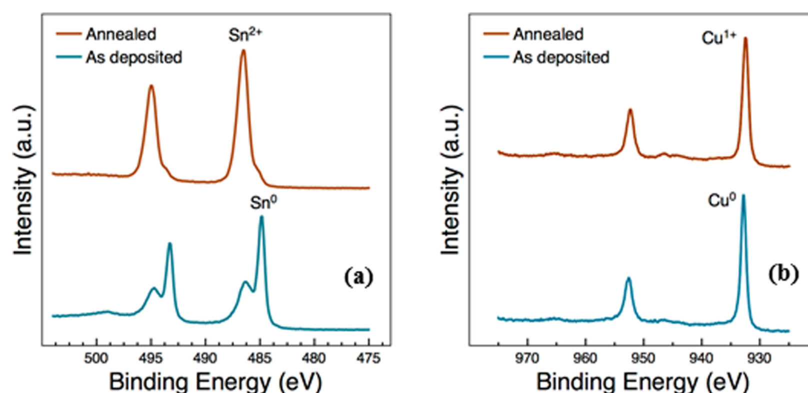

Figure 3. XPS spectrum before and after annealing at 170°C for (a) SnO layer, where a clear phase transformation from Sn−SnO to SnO is observed, and (b) Cu_2O layer with a 0.4 eV downward shift after annealing.

its spin-orbit doublet peaks of Sn 3d core level before and after annealing as shown in Figure 3a. For the as-deposited films, the XPS analysis (measured after 180 s etching), showed the presence of SnO phase, identified by peaks at 486.5 (Sn^{2+} $3d_{5/2}$) and 495.1 eV (Sn^{2+} $3d_{3/2}$).[18] In addition, two sharp peaks, centered at 484.9 (Sn^0 $3d_{5/2}$) and 493.5 eV (Sn^0 $3d_{3/2}$), were observed indicating the existence of 61% of metallic Sn in the film. This high percentage of Sn is expected for 3% O_{pp} SnO films. However, the post-annealed sample showed a dominant SnO phase with small amounts of the metallic phase remaining (~6 at %).

The spectra of Cu 2p before and after annealing (after 60s Ar^+ etching) are shown in Figure 3b. Prior to annealing, a 932.8 eV binding energy, corresponding to metallic Cu,[19] is observed. After annealing, a 0.4 eV downward shift of the Cu $2p_{3/2}$ binding energy from 932.8 to 932.4 eV occurs. The 932.4 eV binding energy corresponds to Cu_2O phase,[20] which shows that annealing leads to more oxidized copper oxide film. In both Cu 2p spectra, no traces of (2+) oxidation state of Cu (Cu^{2+} $2p_{3/2}$ peak at 933.76 eV) are identified.

The observation that copper oxide films become more oxygen rich after annealing was confirmed by additional data. XPS results showed that without Ar^+ etching, the Cu $2p_{3/2}$ peak in the as-deposited film is situated at 932.4 eV, which corresponds to Cu_2O phase.[20] In comparison, for the annealed film the Cu $2p_{3/2}$ peak is shifted to 933.7 eV and the Cu 2p shows additional satellite peaks (938-946 eV) corresponding to CuO phase[20] (results not shown). Thus, we can conclude that annealing in air induces further surface oxidation of the copper oxide film and diffusion of oxygen through the thin film occurs leading to an oxygen enriched copper oxide (Cu_2O) film, even as copper oxide transports oxygen to the underlying SnO film.

Additionally, Figure 4a shows a cross-sectional TEM image taken from the 10/15 nm stack annealed at 170°C. The enlarged image of the channel, Figure 4b, verifies that it consists of two separate layers with different microstructures. This feature confirms the previous XPS results that, even after annealing, the active channel of our bilayer TFT still comprises the Cu_2O and SnO as two separate layers. To check how transparent our Cu_2O/SnO channel was, the optical transmittance for the sample having the optimal thickness ratio (t_{Cu_2O}/t_{SnO} = 10/15) deposited on a glass substrate was measured. An average transmittance of 66% in the optical range (400−700 nm) is observed.

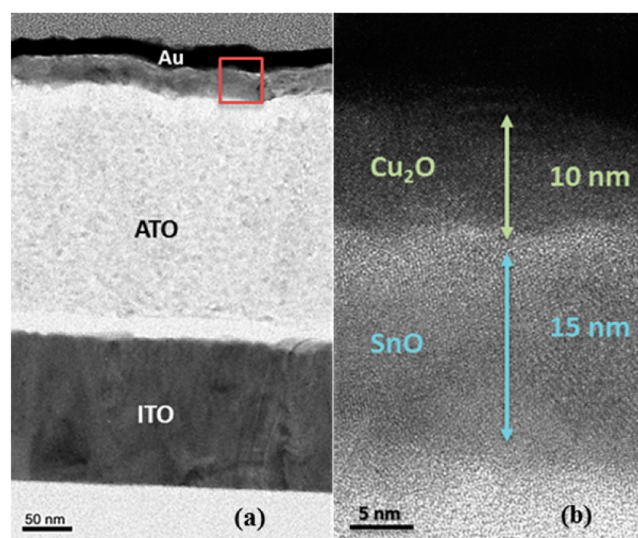

Figure 4. (a) Cross-section TEM micrograph taken from t_{Cu_2O}/t_{SnO} = 10/15 bilayer TFT annealed at 170°C. (b) Enlarged image from the area marked by a square in panel a.

CONCLUSIONS

In summary, we have developed transparent, p-type Cu_2O/SnO bilayer channel TFTs with tunable device performance. By controlling the thickness of each layer, we could tune the required process temperature and device performance. SnO phase formation could be manipulated not only by sputter process condition, but also by controlling oxygen diffusion from Cu_2O capping layer into the underlying SnO_x film. Our t_{Cu2O}/t_{SnO} = 10/15 nm bilayer TFT showed a good p-type operation with a field-effect mobility, off-current, and threshold voltage of 0.66 cm^2/V s, 6.63 nA, and −5.2 V, respectively.

AUTHOR INFORMATION

Corresponding Author

*E-mail: husam.alshareef@kaust.edu.sa.

Notes

The authors declare no competing financial interest.

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